Department of Computer Science & Technology

10th Meeting - Board of Studies (Online)

Minutes of Meeting

10th BoS - Computer Science & Technology meeting was held online on Gmeet Platform at 12.30 on 21st Feb 2023

MEMBERS PRESENT:

1.	**Prof. Anjana Gosain, Professor, GGSIP University**	**Expert Member**
2.	**Dr. Manpreet Kaur, Professor and Head**	**Chairperson**
3.	**Dr. Jyoti Pruthi, Professor**	**Member**
4.	**Dr Susmita Ray, Professor**	**Member**
5.	**Dr. Sachin Lakra, Professor**	**Member**
6.	**Dr. Parneeta Dhaliwal, Professor**	**Member**
7.	**Dr. Mrinal Pandey, Professor**	**Member**
8.	**Ms. Chandni Magoo, Associate Head**	**Special Invitee**
9.	**Dr. R. Girija, Associate Professor**	**Special Invitee**
10.	**Dr. Mamta Arora, Associate Professor**	**Special Invitee**
11.	**Dr. Neelu Chaudary, Associate Professor**	**Special Invitee**

Following two members excused themselves for not attending the meeting due to their unavoidable engagements:

1. Ms. Priyanka, Analysis Director, Dunnhumby Special Invitee, Alumnus Member
2. Mr. Amitava Chakraborty Sr. Architect IBM Infrastructure Services, Special Invitee, Industry Expert

At the outset, the chairperson welcomed all the board members, for sparing the time from the busy schedule to attend the meeting. After that agenda items were taken and the board recommended as under:

Agenda Points discussed and decisions arrived at are mentioned below:

10.1 Confirmation of the MOM of the 9th BOS held on 26th July 2022.

The chairperson presented the previous BOS which was conducted on 26th July 2022 and informed that all decisions have been smoothly implemented as per the discussions.

10.2 Approval of Program Specific Outcomes (PSO) and Program Structure (1st Year) B.Tech

Robotics & AI Program

The chairperson presented the following two proposed Program Specific Outcomes of the new course B.Tech – Robotics and AI for the approval of the board as below.

PSO 1: Design the robotic structure for different applications by applying fundamentals of Electronics, Electrical, Mechanical & Computer Science & Engineering

PSO 2: Develop skills to solve industrial & social challenges with Artificial Intelligence enabled robots ensuring standards and ethics.

The program structure of 1st year of B.Tech- Robotics and AI was also presented before the members of the board. The expert member raised her concern that 2nd semester is heavy in terms of credits .

Decision:

The chairperson gave justification that credits are on a higher side as it is an interdisciplinary course which is designed at the intersection of Computer engineering, Electronics engineering and Mechanical engineering. The program structure of B.Tech- Robotics and AI has been discussed in **Annexure-A.**

10.3 Approval of Course Assessment Plans for Jan-July 2023 session

The Chairperson presented the Course Assessment plans for all the courses as proposed by the course coordinator faculty for the Jan 2023 - June 2023 session.

Decision: - BOS approved Course Assessment plans of all the courses for July-December 2022-23 sessions.

10.4 Approval of the list of all courses being offered in PBL (Project-based learning) mode for the Jan-July 2023 session.

The Chairperson presented the courses which are proposed to be offered in **Project-Based Learning** mode are listed below,

Subject in PBL Mode	**Subject Code**	**Credits**	**Semester**	**Course Coordinator/ Subject Faculty**
Modern Architecture Patterns	CSH322B-T&P	5	6	Dr. Sanjay Singh
Natural Language Processing	CSH324B-T&P	5	6	Ms. Priyanka Gupta
Unsupervised Learning and Neural Network	CSH213B-T&P	5	4	Dr. Mrinal Pandey
Cloud Computing	CSH404B-T &P	5	6	Dr. Shalu
Big Data	CSH402B-T&P	4	6	Ms.Anupriya Sharma
Object Oriented Software Engineering	CSH316B-T&P	4	6	Dr. Vandana BHasin

The expert put forth their interest to see the list of projects which are offered to the students.

Decision: - It was shared that a list of reference problem statements is shared with students but they have flexibility to choose their own problem statement. Also, they are motivated to choose problem statements which are aligned with one or more SDGs

10.5 Updation of Credits for Professional Communication I, Professional Communication II, Professional Competency Enhancement I and Professional Competency Enhancement II

Chairperson shared that the minor modifications in credits of a few courses such as Professional Communication I & II, Professional Competency Enhancement-III and IV, were needed for placement preparation of students. L-T-P's and credits are revised as per the no. of hours of teaching.

Sl.No.	Program	Course Code	Course Name	Sem	L-T-P	Credits
1	B.Tech (CSE)	CDO105	Professional Communication I	2	2-0-0	1
2	B.Tech(CSE)	CDO106	Professional Communication-II	2	2-0-0	1
3	B.Tech (CSE)	CDO202	Professional Competency Enhancement-II	4	4-0-0	2
4	B.Tech (CSE)	CDO302	Professional Competency Enhancement-IV	6	4-0-0	2

Decision: BOS approved the credits and L-T-P mode for above courses.

10.6 Assessment of CO attainment and corresponding actions taken for all courses of July-December 2022 session.

Chairperson presented assessment of CO attainment of all courses and actions taken of July -Dec 2022 Session as shown in Annexure-B. Few observations and corresponding actions taken are given below:

Observations:

Most of the courses attained a level varying **around 2;** a few courses have attained **Level 3**, whereas a few courses were able to score **Level 1 only**.

Actions:

1. For courses attaining Level 1, it was decided to improve the **quality of assignments, course content, tutorials and lab exercises** so that learners are able to perform better in the next academic cycle.
2. Similarly, it was advised to lay more emphasis on fundamental concepts, so as to have before proceeding to advanced topics.
3. For courses meeting their attainment levels, it may be decided by faculty members **to increase the CO attainment targets** in the next academic cycle, or to increase the competency level of the course.

Decision: The expert advised to analyze the observations carefully and to decide future course of actions so as to meet/improve the target levels.

10.7 Approval of list of online courses from online platforms: Infosys-SpringBoard and SWAYAM-NPTEL which are being offered for credit transfer for Jan-June 2023 academic session.

The list of MOOC courses that have been shortlisted by Deptt. Review Committee for credit transfer for the upcoming semester on the following platforms was presented for approval. The list has been attached as **Annexure-C.**

It was shared with the board members that it is mandatory for the students of 2k21-2k25 batch and subsequent batches to complete two MOOC courses for credit transfer as per the ordinance. Also, it was shared that 115 students have registered for NPTEL and Infosys SpringBoard courses.

Decision: BOS approved all the online courses which are planned to be offered to the students**.**

10.8 Approval of list of external examiners for Project Based Learning (PBL) courses and practical examinations

List of external examiners for practical and also for PBL mode courses were proposed as shown in **Annexure - D.**

Decision: - All external examiners for practical examination and PBL courses have been approved.

10.9 Revision of syllabus of course: Data structures and Algorithms (Code: CSH-103B T & P, Semester-II)

Chairperson proposed the revision of the course “Data structures and Algorithms” semester-II, as given below.

The following changes have been proposed in the syllabus:

1. Rearrangement of topics related to Searching, Sorting, Arrays, pointers, Linked list for better flow of understanding of students.
2. Priority Queues- Implementation Concepts have been added in the syllabus.
3. It has been proposed to B+ trees to be removed from the DSA syllabus so as to concentrate more

on Binary Search Trees and further to add B+ trees in Analysis and Design of Algorithms.

4. Instead of Connected components topic, shortest path algorithms have been added in the course.

Decision: BOS approved the proposed revisions in Data structures and Algorithms syllabus (CSH103B-T&P).

10.10 Approval for award of credits as per the Policy for Additional Internship

Chairperson shared with the committee about number of credits awarded to students: Karan Aaditya Ghoshal (2K19CSUN01026)**-approved-9th BOS)**, Sarthak Rastogi (2K19CSUN04024), Aayush Kumar Singh(2K19CSUN01123), Chetna Batra (2K19CSUN01129) from the CST department who started their internships in 7th Semester in industry through the Policy for Additional Internship.

Decision: The credits availed through internships during the semester against Additional Internship Policy were approved as mentioned in Annexure E.

10.11 Revision of Course: Digital Electronics & Microcontrollers- ECH308B-T

The Chairperson shared that the course titled "Digital Electronics and Microcontroller" is quite complicated due to the combination of two completely independent and unrelated courses which makes it difficult to understand for B.Tech. CSE Students. Consequently, the academic performance of the students in this course has been quite low. The same feedback has been given by the faculty members from the ECE department. Therefore, it has been decided to split the course into two individual courses as "Digital Electronics" and "Microcontroller & Interfacing" so as to justify the course in a better manner.

Decision; BOS approved the splitting of the course "Digital Electronics & Microcontrollers" into two individual courses. This decision was made after careful consideration that the existing course was not adequately meeting the needs and expectations of the students..

10.12 Introduction to New initiatives: Technical training, IEEE Robotics & Automation Society

Chairperson proudly mentioned about establishing a new professional society chapter named "IEEE ROBOTICS & AUTOMATION Society" in our department. The vision and Mission of this society is given below,

Decision: The expert appreciated this initiative and discussed the events that should be planned under this society.

10.13 Faculty and Student Achievements.

Students are participating in many events such as INNOSKILL, HACK-A-THON, IEEE events, research paper publications, industry initiatives etc. Many of our faculties published the research papers in SCI and scopus indexed journals and conferences, filed the patents and copyrights, delivered expert talks and acted as session chairs, keynote speakers in many workshops and conferences. Few faculty members are acting as editors/guest editors/ reviewers in many esteemed journals. The BOS experts appreciated the way the department is progressing and taking initiatives for the professional development of the students

and up skilling of the faculty members.

The meeting ended with the thanks to BOS expert members for their valuable time and suggestions.

Prepared by:

Dr. R Girija,
Associate Professor, CST

Approved by:
BOS Chairperson,

Dr. Manpreet Kaur
Head, CST

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Department of Computer Science & Technology
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Faridabad-121001

Annexure - A

B-TECH ROBOTICS AND ARTIFICIAL INTELLIGENCE							
SEMESTER - 1							
NOMENCLATURE AS PER AICTE	**SUBJECT CODE**	**SUBJECT NAME**	**L**	**T**	**P**	**NO. OF CONTACT HOURS PER WEEK**	**NO. OF CREDITS**
ENGINEERING SCIENCE COURSES	CSH101B-T/P	PROGRAMING FOR PROBLEM SOLVING USING C	3	1	2	6	5
PROGRAM CORE COURSES	CSH107B-T/P	OVERVIEW OF DATA SCIENCE & MACHINE LEARNING	3	1	2	6	5
ENGINEERING SCIENCE COURSES	ECH103B-T/P	BASICS OF ELECTRONICS AND ELECTRICAL ENGINEERING	3	1	2	6	5
PROGRAM CORE COURSES	MEH108B-T/P	INTRODUCTION TO ROBOTICS	3	0	2	5	4
ENGINEERING SCIENCE COURSES	MEW106B	COMPUTER AIDED DRAFTING	0	0	2	2	1
BASIC SCIENCE COURSES	PHH101B-T/P	QUANTAM MECHANICS FOR ENGINEERS	3	1	2	6	5
	CDO105	PROFESSIONAL COMMUNICATION-I	2	0	0	2	1
TOTAL (L-T-P/CONTACT HOURS/CREDITS)			**15**	**4**	**12**	**31**	**26**
SEMESTER - 2 (ROBOTICS and AI)							
NOMENCLATURE AS PER AICTE	**SUBJECT CODE**	**SUBJECT NAME**	**L**	**T**	**P**	**NO. OF CONTACT HOURS PER WEEK**	**NO. OF CREDITS**
ENGINEERING SCIENCE COURSES	CSH103B-T	DATA STRUCTURES & ALGORITHMS	3	1	0	6	5
	CSH103B-P	DATA STRUCTURES & ALGORITHMS LAB	0	0	2		
PROGRAM CORE COURSES	CSH108B-T	PYTHON PROGRAMMING	3	1	0	4	5
	CSH108B-P	PYTHON PROGRAMMING LAB	0	0	2	2	
PROGRAM	MEH109B-	MATERIALS FOR	3	0	0	5	4

CORE COURSES	T	ROBOTICS					
PROGRAM CORE COURSES	MEH109B-P	MATERIALS FOR ROBOTICS LAB	0	0	2		
PROGRAM CORE COURSES	ECH110B-T	DIGITAL LOGIC AND HARDWARE DESIGN	3	1	0	6	5
PROGRAM CORE COURSES	ECH110B-P	DIGITAL LOGIC AND HARDWARE DESIGN LAB	0	0	2		
PROGRAM CORE COURSES	ECW218B	SENSORS, ACTUATORS AND AUTOMATION (ARDUINO, R-PI ETC)	0	0	2	2	1
BASIC SCIENCE COURSES	CHH144-T/P	CHEMISTRY-I	**3**	**0**	**2**	**5**	**4**
	CDO106	PROFESSIONAL COMMUNICATION-II	2	0	0	2	1
TOTAL (L-T-P/CONTACT HOURS/CREDITS)			**11**	**2**	**12**	**32**	**25**

Annexure -B

Subject	CO1	CO2	CO3	CO4	CO5	CO6	Overall CO attainment
SPM	2	2	3	3	3	NA	2.6
BUSINESS INTELLIGENCE & ANALYTICS WITH R	2	3	3	3	NA	NA	2.75
BUSINESS INTELLIGENCE & ANALYTICS WITH R	3	3	3	3	NA	NA	3
R Programming	3	3	3	3	NA	NA	3
Analysis and Design of Algorithm 3RD SEM/AIML 5TH SEM-pp	1	1	1	1	1	NA	1
Analysis and Design of Algorithm 3RD SEM/AIML 5TH SEM-pr	3	3	3	3	3	NA	3
USER INTERFACE-II	1	1	2	3	NA	NA	1.75
Virtualization - Containers/Cloud	1	1	1	1	NA	NA	1
Operating system	3	3	2	3	NA	NA	2.75
Operating system	2	2	2	2	NA	NA	2
Programming for problem solving using C	3	3	3	3	NA	NA	3
	3	3	3	3	NA	NA	3
Theory of Automata & Compiler Design	2	2	3	2	3	NA	2.4
Theory of Automata & Compiler Design	2	3	3	1	2	NA	2.2
Continuous Integration & Continuous Depolyment	3	3	3	2	1	NA	2.4
Version Control and Automation	2	3	3	1	2	NA	2.2
Data structures and Algorithms	2	2	2	2	NA	NA	2
Data structures and Algorithms	3	3	3	3	NA	NA	3
Database management system	3	3	3	1	NA	NA	2.5
Database management system lab	2	2	1	2	1	NA	1.6
Computer Vision and Data Visualization	3	2	3	3	NA	NA	2.75
Computer Vision and Data Visualization	0	3	1	0	NA	NA	1
Advance Neural Network	3	1	3	3	3	NA	2.6
Advance Neural Network	3	3	3	3	2	NA	2.8

INFORMATION RETRIEVAL	3	2	3	3	NA	NA	2.75
Big Data	1	1	1	1	NA	NA	1
System & Network Administration	1	1	1	1	2	NA	1.2
Big Data	2	2	2	2	NA	NA	2
Software Requirements Engineering	2	2	3	2	NA	NA	2.25
ADVANCED ALGORITHMS	1	1	1	1	1	NA	1
ADVANCED ALGORITHMS	2	2	2	2	1	NA	1.8
OOPs using Java	1	1	1	3	NA	NA	1.5
Computer Architecture and Organisation	2	2	3	3	NA	NA	2.5
Computer Architecture and Organisation Lab	1	1	1	1	1	NA	1
Network Security	1	1	3	3	NA	NA	2
Network Security lab	2	1	3	3	NA	NA	2.25
Advanced Java	3	3	1	3	3	NA	2.6
Data Visualization using Tableau	3	3	3	3	3	NA	3
GREEN COMPUTING	3	2	2	1	2	NA	2
Mobile Computing with Android	3	2	1	1	1	3	1.83
Image Editing & Animation	3	3	2	2	NA	NA	2.5
User Experience	3	3	3	3	NA	NA	3
Computer Networks	3	3	3	3	3	NA	3
Computer Networks Lab	3	3	3	3	3	NA	3

Annexure - C

NPTEL courses- (IV Semester)

SNo	Course Type (Domain / Allied Elective)	Discipline	Duration/ Credits at MRU	Mapping Status Full/Partial
1	Soft Allied(1)	Entrepreneurship Essentials	8 weeks/2	Full
2		Design, Technology and Innovation	8 weeks/2	Full
1	Workshop Elective	Programming, Data Structures And Algorithms Using Python	8 weeks/1.5	Full
2		Information Security - 5 - Secure Systems Engineering	8 weeks/1.5	Full
3		Programming in C++	8 weeks/1.5	Full
4		Data Science for Engineers	8 weeks/1.5	Full
5		Cloud Computing and Distributed Systems	8 weeks/1.5	Full
6		User-centric Computing for Human-Computer Interaction	8 weeks/1.5	Full
7		Data Mining	8 weeks/1.5	Full
9		Cloud computing	8 weeks/1.5	Full
1	Allied(1)	Entrepreneurship Essentials	8 weeks/2	Full
2		Design, Technology and Innovation	8 weeks/2	Full
1	Allied(2)	Patent Law for Engineers and Scientists	12 Weeks/2	Full
2		Ethics In Engineering Practice	8 Weeks/2	Full

SNo	Course Type (Domain / Allied Elective) Hard/Workshop	Infosys Springboard Course	Duration (Weeks)
1	Domain Elective	Foundational Data Science	12
2		API and Microservices	12
3		.NET Full Stack Developer	12
4	Elective Workshop -1	Citizen Data Science using Python	8

5		Agile Software Development using Scrum	8
6		Foundation of Cyber Security	8
7		Angular Developer	8

Annexure –D

	Old Syllabus	Revised Syllabus
	Unit 1 Introduction to Data structure Concept of data structure, choice of right data structures, types of data structures, Abstract Data types, , Introduction to algorithms, how to design and develop an algorithm: stepwise refinement, algorithm analysis, complexity of algorithms	**Unit 1 Introduction to Data structure** Concept of data structure, choice of right data structures, types of data structures, Abstract Data types Introduction to algorithms, how to design and develop an algorithm: stepwise refinement, algorithm analysis, complexity of algorithms Introduction to pointers, Pointer variables, Pointer and arrays, Array of pointers, pointers and structures, Dynamic allocation.
	Unit 2: Arrays and Linked List: Introduction, One Dimensional Arrays, Two dimensional array, Address Calculation, Array operations defined: traversal, selection, searching, linear search, binary search Sorting Introduction: selection sort, bubble sort, insertion sort ,quick sort, merges sort, Introduction to pointers, Pointer variables, Pointer and arrays, Array of pointers, pointers and structures, Dynamic allocation. Concept of a linked list, Traversing & searching in Link List, Insertion in a linked list,deletion in a linked list, Deletion continue,Doubly linked list:Insertion, Deletion in doubly linked list,circular linked List, Insertion in Circular Link List, deletion in Circular Link List, Concepts of header linked lists. Applications of linked lists.	**Unit 2: Arrays and Linked List** **Arrays**: Introduction, One Dimensional Arrays, Two dimensional array, Address Calculation, Array operations defined: traversal. **Linked Lists**: Concept of a linked list, Traversing & searching in Link List, Insertion in a linked list,deletion in a linked list, Deletion continue,Doubly linked list:Insertion, Deletion in doubly linked list,circular linked List, Insertion in Circular Link List, deletion in Circular Link List, Concepts of header linked lists. Applications of linked lists. **Searching**: Linear search, binary search **Sorting**: Sorting Introduction: selection sort, bubble sort, insertion sort ,quick sort, merges sort
	Unit 3: Stacks and Queues **Stacks**: Introduction to Stacks, array representation of stack, operations on stack: PUSH, POP, Concept of precedence and associativity in	**Unit 3: Stacks and Queues** **Stacks**: Introduction to Stacks, array representation of stack, operations on stack: PUSH, POP, Linked list representation of stack,

	expressions, difficulties in dealing with infix expressions, Resolving precedence of operators and association of operands, postfix & prefix expressions, conversion of expression from one form to other form using stack., Evaluation of expression in infix, postfix & prefix forms using stack ,Linked list representation of stack, Applications of stacks **Queues**, Array representation of Queues, operations on queue: insertion and deletion, Circular queue,operations, priority queues, dequeue, Applications of Queues.	Applications of stacks Concept of precedence and associatively in expressions, difficulties in dealing with infix expressions, Resolving precedence of operators and association of operands, postfix & prefix expressions, conversion of expression from one form to other form using stack., Evaluation of expression in infix, postfix & prefix forms using stack **Queues**, Array representation of Queues, operations on queue: insertion and deletion, Circular queue,operations, introduction to priority queues, dequeue, Applications of Queues.
	Unit 4: Trees and Graphs Trees definition, characteristics concept of child, sibling, parent child relationship etc, binary tree: different types of binary trees based on distribution of nodes: complete binary tree, binary tree (threaded and unthreaded), operation on binary tree: insertion, deletion, searching and traversal of binary trees, traversing: Preorder, Postorder and Inorder, Introduction to binary search tree, operations BST: searching,insertion, Deletion in BST, Introduction to AVL tree: Concept of balanced trees, balance factor in AVL trees, Insertion in AVL ,deletion in AVL deletion in AVL, B tree insertion, deletion, B+ tree insertion, deletion **Graphs**: Definition, Relation between tree & graph, directed and undirected graph, connected and disconnected graph, Representation of graphs using adjacency matrix and list, Depth first and breadth first traversal of graphs, finding connected components,Applications of Graph.	**Unit 4: Trees and Graphs** **Trees**: definition, characteristics concept of child, sibling, parent child relationship etc, binary tree: different types of binary trees based on distribution of nodes: complete binary tree, binary tree (threaded and unthreaded), operation on binary tree: insertion, deletion, searching and traversal of binary trees, traversing: Preorder, Postorder and Inorder, Introduction to binary search tree, operations BST: searching,insertion, Deletion in BST, Introduction to AVL tree: Concept of balanced trees, balance factor in AVL trees, Insertion in AVL ,deletion in AVL, B tree insertion, deletion **Graphs**: Definition, Relation between tree & graph, directed and undirected graph, connected and disconnected graph, Representation of graphs using adjacency matrix and list, Depth first and breadth first traversal of graphs, finding connected components,Applications of Graph.

ANALYSIS AND DESIGN OF ALGORITHMS

	Old Syllabus	**Revised Syllabus**
	Unit 1 INTRODUCTORY CONCEPTS: Growth of Functions, Summations, Algorithm Design Paradigms, Characteristics of Algorithm, Comparing the performance of different algorithms for the same problem, asymptotic notation. Polynomial vs. Exponential running time. Disjoint Set operations, Linked List representation of disjoint sets, disjoint set forests. Insertion sort, Selection sort, Bubble sort, Binary search algorithm and its analysis.	Unit 1 INTRODUCTORY CONCEPTS: Growth of Functions, Summations, Algorithm Design Paradigms, Characteristics of Algorithm, Comparing the performance of different algorithms for the same problem, asymptotic notation. Polynomial vs. Exponential running time. Disjoint Set operations, Linked List representation of disjoint sets, disjoint set forests. Insertion sort, Selection sort, Bubble sort, Binary search algorithm and its analysis.
	Unit 2: Divide and Conquer method: Recurrence relations: Solving Recurrence by substitution method, recurrence tree ,master method; Sorting algorithms such as Merge sort, Quick sort, Heap sort, Radix Sort, Counting Sort, Bucket Sort with analysis of their running times .Strassen's matrix multiplication. Greedy Method: Activity Selection Problem, knapsack problem, job sequencing with deadlines,	Unit 2: Divide and Conquer method: Recurrence relations: Solving Recurrence by substitution method, recurrence tree ,master method; Sorting algorithms such as Merge sort, Quick sort, Heap sort, Radix Sort, Counting Sort, Bucket Sort with analysis of their running times .Strassen's matrix multiplication. Greedy Method: Activity Selection Problem, knapsack problem, job sequencing with deadlines,
	Unit 3: Minimum spanning trees, single source shortest paths, all pairs shortest paths Dynamic Programming: General method, optimal binary search trees, O/I knapsack, the traveling salesperson problem, Matrix chain multiplication, Longest common Subsequence and their analysis.	Unit 3: B+ TREE insertion, deletion, Minimum spanning trees, single source shortest paths, all pairs shortest paths Dynamic Programming: General method, optimal binary search trees, O/I knapsack, the traveling salesperson problem, Matrix chain multiplication, Longest common Subsequence and their analysis,

	Unit 4: Backtracking and Branch & Bound: General method, 8 queen's problem, graph coloring, Hamiltonian cycles, Vertex Cover Problem, analysis of these problems Branch and Bound: Method, O/I knapsack and traveling salesperson problem, efficiency considerations NP hard and NP Complete: NP Hard graph Problems, Cook's Theorem.	Unit 4: Backtracking and Branch & Bound: General method, 8 queen's problem, graph coloring, Hamiltonian cycles, Vertex Cover Problem, analysis of these problems Branch and Bound: Method, O/I knapsack and traveling salesperson problem, efficiency considerations NP hard and NP Complete: NP Hard graph Problems.

1- B+ tree insertion, deletion is deleted from data structure and algorithm syllabus and added into analysis and design of algorithm syllabus.

2- Cook's Theorem is deleted from the syllabus from the last unit.

Annexure –E

Sl.No.	External Examiner	University
1	Mr. Naresh Kumar	SGT University
2	Dr. Kuldeep Tomar	NGF College of Engineering & Technology
3	Dr. Neelam Duhan	J. C. Bose University of Science and Technology, YMCA
4	Dr. Rohit Tanwar	UPES, Dehradun
5	Puneet Garg	ABES ENGG. COLLEGE, GHAZIABAD,U.P.
6	Ms. Sarika	IMS Engineering College, GHAZIABAD,U.P.
7	Ms. Dimple	J. C. Bose University of Science and Technology, YMCA
8	Dr. Harish	J. C. Bose University of Science and Technology, YMCA
9	Mohit Chowdhary	Galgotias College of Engineering
10	AMIT RAJPUT	J. C. Bose University of Science and Technology, YMCA, Sector 6, Faridabad, Haryana
11	Naved Alam	Jamia hamdard University
12	Sushil Chhabra	IMT FARIDABAD ,SECTOR 86,FBD
13	Dr. Mala Saraswat	Bennett University, Greater Noida
14	Ms. Ranjita Joon	Nehru Govt. College, Faridabad
15	Dr. Neeraj Varshney	GLA University,Mathura

ANNEXURE E

Course Title/Code	**DIGITAL ELECTRONICS**
Course Type:	**Core**
Course Nature:	**Hard**
L-T-P-O Structure	**3-1-2-0**
Objective	**To understand the logic of various digital circuits which will further help in their designing.**

Section-A

Fundamentals of Digital Techniques: Binary, Octal and Hexadecimal number system, Binary, Octal and Hexadecimal arithmetic, Radix conversion, Signed binary numbers, Fixed and floating point numbers, BCD, Gray, Excess-3, Self-Complimentary codes, Error detecting and correcting codes- Parity check codes, Hamming code, Basic logic operation and logic gates, Truth table, Fundamental theorems of Boolean Algebra, Standard representation of logic functions-SOP and POS forms, Simplification using K-map and QuineMc- Clusky methods.

Section-B

Combinational Design using MSI Devices: Design of combinational circuits - Half, full and parallel adder, Half and full subtractor, BCD adder, BCD Adder as a Subtractor, Multiplexer, Demultiplexer, Decoder/display driver, Encoder, Priority encoder, Magnitude comparator, Code converter, Binary Multiplier, Design examples.

Section-C

Sequential Logic Circuits: Latches, Flip-flops: R-S, J-K, Master-slave, T, D, Conversion of flip flops, Registers: SISO, SIPO, PISO, PIPO, Bidirectional and Universal registers, Counters: Asynchronous, Synchronous counters, Shift register counters: Ring & Johnson Counter, Designing examples of Counters, Arithmetic logic unit.

Section-D

Memory and Programmable Logic Devices: RAM, ROM, PROM, PLA, PAL, FPGA, CPLD, Introduction to Digital Logic Families: RTL, DTL, DCTL, HTL, TTL, ECL, MOS and CMOS logic families, Tristate logic, Principle of A/D Convertors & its types

List of Experiments:

1. **Verification of truth table of logic gates using TTL ICs, designing gates using diodes & resistors.**
2. **Design of AND, OR, NOT gates using Universal Gates.**
3. **Implementation of SOP & POS Boolean Functions.**
4. **Design a function using K-map and verify its performance using SOP and POS form**
5. **Design of Combinational circuits- Adders & Adder as Subtractor**
6. **Design of Combinational circuits- MUX and DEMUX.**
7. **Design a binary to gray code converter and BCD to excess-3 converter**
8. **Design of Arithmetic Logic Unit (ALU)**
9. **Analysis of basic flip-flops. Design a shift register using flip-flops**
10. **Design a modulus N counter and a ring counter**
11. **Mini Project**

Text Books:

1. **M. Morris Mano and M. D. Ciletti, Digital Design, 4th Edition, Pearson Education**
2. **Anand Kumar, Fundamentals of Digital Circuit, PHI Publication**

Reference Books:

1. **Thomas L. Flyod, Digital Fundamentals, Pearson Education India**
2. **R.P. Jain, Modern digital electronics, 3rd edition, TMH Publication.**

Digital Electronics and Microcontroller

Section A

Boolean algebra and Combinational Circuits

BCD numbers, BCD addition and subtraction.De Morgan's theorem, standard POS and SOP forms, min-term and max-term representation of Boolean functions, simplification of Boolean functions using K-maps. Half and Full adders, Half and Full Subtractor, Multiplexer, Demultiplexer, Encoder, Decoder, Priority Encoder, Magnitude comparator, Code converter, Binary Multiplier

Section B

Sequential Circuits

Latches, R-S, J-K and Master-Slave, T and D flip flops, Conversion of flip flops, Shift registers, Ring counter, Ripple and Synchronous counter, Modulo-N counter, Decade counters, Digital to Analog converter (binary weighted register and ladder types) and Analog to Digital converter (using D/A converter and comparator),

Section C

8051 MICRO CONTROLLER

Architecture of 8051 – Signals – Operational features – CPU, ALU, address, data and control bus, Working registers, SFRs, Clock and RESET circuits, Stack and Stack Pointer, Program Counter, I/O ports, Memory Structures, Data and Program Memory, Addressing mode, 8051 Instruction set, Instruction timings. Data transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Subroutine instructions, Bit manipulation instruction, Assembly language programs.

Section D

Interfacing Microcontroller

Programming 8051 Timers – Serial Port Programming – Interrupts Programming – LCD and Keyboard Interfacing – ADC, DAC and Sensor Interfacing – External Memory Interface- Stepper Motor and Waveform generation

Case studies: Traffic Light control, LED display , LCD display, Keyboard display interface and Alarm Controller.

Course Title/ Code	**MICROCONTROLER & INTERFACING**
Course Type:	**Core (Departmental)**
Course Nature:	**Hard**
L-T-P-O Structure	**(3-1-2-0)**
Objectives	**Students will be able to build microcontroller based system around 8051 and PIC.**

Section-A

INTRODUCTION OF MICROCONTROLLER: Different types of microcontrollers: Embedded microcontrollers, External memory microcontrollers; Processor Architectures: Harvard V/S Princeton, CISC V/S RISC; microcontrollers memory types; microcontrollers features: clocking, i/o pins, interrupts, timers, peripherals.

Section-B

MICROCONTROLLER ARCHITECTURE: Introduction to PIC microcontrollers, Architecture and pipelining, program memory considerations, Addressing modes, CPU registers, Instruction set, simple operations.

Section-C

Microcontrollers - Microcontroller 8051- Architecture, Pin Diagram, I/O Ports, Internal RAM and Registers, Interrupts, Addressing Modes, Memory Organization and External Addressing, Instruction Set, Assembly Language Programming, Real Time Applications of Microcontroller- Interfacing with LCD, ADC, DAC, Stepper Motor, Key Board and Sensors.

Section-D

Embedded Systems-Introduction, Classification, Processors, Hardware Units, Software Embedded into System, Applications and Products of Embedded Systems, Structural Units in Processor, Memory Devices,

I/O Devices, Buses, Interfacing of Processor Memory and I/O Devices, Case Study of an Embedded System for a Smart Card.

List of Experiments:

01. Write Assembly language Program to generate 10 kHz square wave Using PIC

02 Study and analysis of interfacing of LCD using PIC controller

03 Study and interfacing of IR (RC5 protocol) and RF Communication using PIC controller

04 To interface PWM based voltage regulator using PIC Microcontroller

05 To study Programming and Transmission & reception of data through Serial port between two PC & study of Parallel printer port using PIC.

06 Write an Assembly language Program to generate 10 kHz square wave Using 8051

07 To study implementation & interfacing of Display devices Like LCD, LED Bar graph & seven segment display with Microcontroller 8051/AT89C51

08 To study implementation & interfacing of Different motors like stepper motor, DC motor & servo Motors. 8051

09. Write an ALP for temperature & pressure measurement 8051.

10. To study Programming and Transmission & reception of data through Serial port & study of Parallel printer port. 8051

Text Books:

1. B. B. Brey: The Intel Microprocessors, Architecture, Programming and Interfacing, Pearson Education.

2. Design with PIC Microcontrollers by John B. Peatman , Pearson.

3. Raj Kamal: Embedded Systems- Architecture, Programming and Design, TMH, New Delhi.

4. V. Udayashankara and M. S. Mallikarjunaswamy: 8051 Microcontroller, TMH, New Delhi.

5. Mazidi and Mazidi: The 8051 Microcontroller and Embedded Systems, Pearson Education.

6. A. V. Deshmukh: Microcontroller (Theory and Application), TMH.

7. D. V. Hall: Microprocessors and Interfacing, TMH

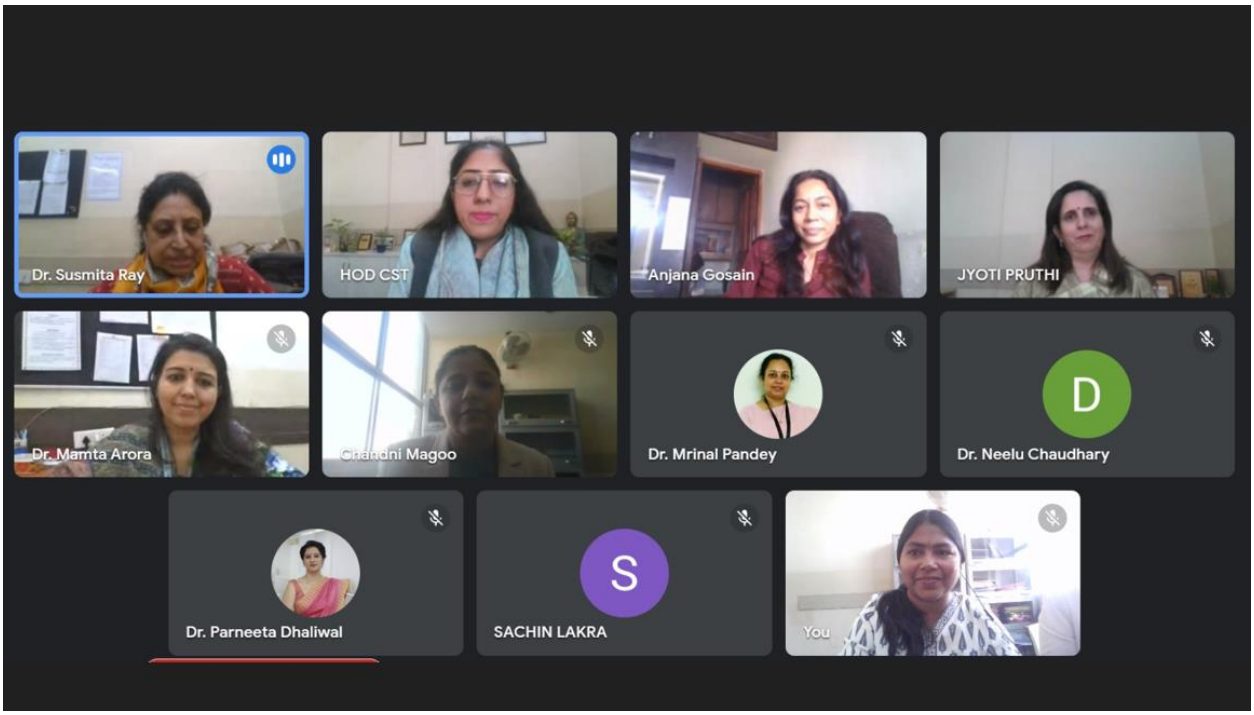
8. Programming and Customizing the 8051 Microcontroller : Predko ; TMH.

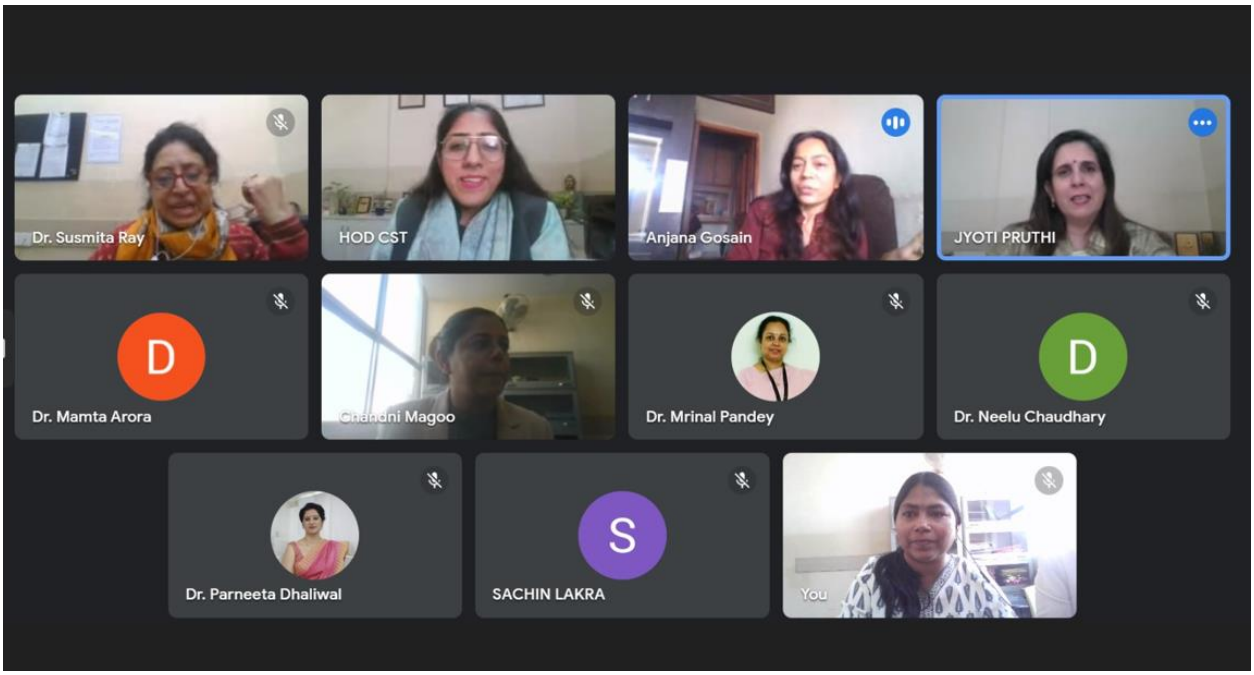
9. Programming Embedded Systems in C and C++ : Michael Barr; SHROFF PUB. & DISTR

ANNEXURE F
Internship Policy

Subject Code	Subject Names	Credits	Student Name
CSN414B	PROJECT	11.5	1. AAYUSH KUMAR SINGH (2K19CSUN01123), 2. CHETNA BATRA (2K19CSUN01129), 3. KARAN AADITYA GHOSHAL (2K19CSUN01026)
CSN415B	PROJECT	21	1. SARTHAK RASTOGI (2K19CSUN04024)

Few Glimpses of 10th BOS meeting


Dr. Susmita Ray
HOD CST
Anjana Gosain
JYOTI PRUTHI
Dr. Mamta Arora
Chandni Magoo
Dr. Mrinal Pandey
D
Dr. Neelu Chaudhary
Dr. Parneeta Dhaliwal
S
SACHIN LAKRA
You


Dr. Susmita Ray
HOD CST
Anjana Gosain
JYOTI PRUTHI
D
Dr. Mamta Arora
Chandni Magoo
Dr. Mrinal Pandey
D
Dr. Neelu Chaudhary
Dr. Parneeta Dhaliwal
S
SACHIN LAKRA
You